LISTING OF THE CLAIMS

No amendments have been made to the claims. The following listing of claims is set forth for convenience of reference.

LISTING OF CLAIMS

1. (previously presented) In a computer having a peripheral component interconnect (PCI) system having a host bridge coupling a plurality of PCI slots of a PCI bus to a processor, the computer accessing base address registers with firmware, a method of identifying a failing PCI slot, comprising the steps of:

(a) creating a firmware maintained PCI resource allocation map in which addresses for PCI slots associated with the base address registers and sizes of address ranges for these addresses are mapped;

(b) updating the firmware maintained PCI resource allocation map upon the occurrence of the firmware being called to execute at least one of a hot plug operation and a PCI configuration space transaction; and

(c) upon the host bridge logging an error address due to a failing PCI slot, identifying the failing PCI slot from the information in the firmware maintained PCI resource allocation map.

2. (original) The method of claim 1 wherein upon the occurrence of a hot plug operation for a PCI slot, a hot plug flag associated with that PCI slot is set and upon the host bridge logging an error address, invalidating the firmware maintained PCI resource allocation map entries associated with each PCI slot having its hot plug flag set.

3. (previously presented) The method of claim 2 and further including upon the occurrence of firmware being called to execute a PCI configuration space transaction, invalidating the firmware maintained PCI resource allocation map entries associated with each PCI slot having its associated hot plug flag set and clearing each such set hot plug flag.

4. (previously presented) The method of claim 1 wherein the step of identifying the failing PCI slot from the information in the firmware maintained PCI resource allocation map includes identifying the failing PCI slot from an address associated with a base address register when the logged error address falls within a known address size range for the address associated with that base address register.

5. (original) The method of claim 4 wherein the step of identifying the failing PCI slot further includes identifying the failing PCI slot as unknown when the logged error address falls after a known address size range of an address associated with that base address register preceding the logged error address.

6. (previously presented) The method of claim 4 wherein the step of identifying the failing PCI slot further includes identifying the failing PCI slot from the address associated with that base address register preceding the logged error address when the address the size range for that preceding base address register is unknown.

7. (previously presented) The method of claim 6 wherein the step of identifying the failing PCI slot further includes identifying the failing PCI slot from the address associated with that base address register preceding the logged error address when the address size range for the address associated with that preceding base address register is unknown.

8. (previously presented) The method of claim 7 wherein upon the occurrence of a hot plug operation for a PCI slot, a hot plug flag associated with that PCI slot is set and upon the host bridge logging an error address, invalidating the firmware maintained PCI resource allocation map entries associated with each PCI slot having its hot plug flag set and clearing each such set hot plug flag.

9. (previously presented) The method of claim 8 and further including upon the occurrence of firmware being called to execute a PCI configuration space transaction, invalidating the firmware maintained PCI resource allocation map entries associated with each PCI slot having its associated hot plug flag set and clearing each such set hot plug flag .

10. (previously presented) In a computer having a peripheral component interconnect (PCI) system having a host bridge coupling a plurality of PCI slots of a PCI bus to a processor, the computer accessing base address registers with firmware, a method of identifying a failing PCI slot, comprising the steps of:

(a) creating a firmware maintained PCI resource allocation map in which addresses for PCI slots associated with the base address registers and sizes of address ranges for these addresses are mapped;

(b) upon the occurrence of a hot plug operation for a PCI slot, setting a hot plug flag associated with that PCI slot;

(c) upon the occurrence of at least one of the firmware being called to execute a PCI configuration space transaction and the host bridge logging an error address, invalidating the firmware maintained PCI resource allocation map entries for each PCI slot having its hot flag set; and

(d) upon the host bridge logging an error address due to a failing PCI slot, identifying the failing PCI slot from an address associated with a base address register when the logged error address falls within a known address size range for the address associated with that base address register and identifying the failing PCI slot as unknown when the logged error address falls after a known address size range of an address associated with that base address register preceding the logged error address.

11. (previously presented) The method of claim 10 wherein the step of identifying the failing PCI slot further includes identifying the failing PCI slot from the address associated with that base address register preceding the logged error address when the address size range for the address associated with that preceding base address register is unknown.

12. (original) In a computer having a peripheral component interconnect (PCI) system having a PCI to PCI bridge coupling a plurality of PCI slots of a PCI bus to a processor, the computer accessing base address registers with firmware, a method of identifying a failing PCI slot below the PCI to PCI bridge, comprising the steps of:

(a) creating a firmware maintained PCI resource allocation map in which addresses for PCI slots associated with the base address registers and sizes of address ranges for these addresses are mapped;

(b) upon the occurrence of a hot plug operation for a PCI slot, setting a hot plug flag associated with that PCI slot;

(c) upon the occurrence of at least one of the firmware being called to execute a PCI configuration space transaction and the PCI to PCI bridge logging an error address, invalidating the firmware maintained PCI resource allocation map entries for each PCI slot having its hot flag set; and

(d) upon the PCI to PCI bridge logging an error address due to a failing PCI slot, identifying the failing PCI slot from an address associated with a base address register when the logged error address falls within a known address size range for the address associated that base address register and identifying the failing PCI slot as unknown when the logged error address falls after a known address size range of an address associated with that base address register preceding the logged error address.

13. (previously presented) The method of claim 12 wherein the step of identifying the failing PCI slot further includes identifying the failing PCI slot from the address associated with that base address register preceding the logged error address when the address size range for the address associated with that preceding base address register is unknown.